REMARKS/ARGUMENTS

These remarks are made in response to the Office Action of November 1, 2007 (Office Action). As this response is timely filed within the 3-month shortened statutory period, no fee is believed due. However, the Examiner is expressly authorized to charge any fees to maintain the pendency of this application to Deposit Account No. 50-0951.

In the Office Action, claims 1, 3, 5-7, 9-11, 17, 19, 21-23, and 25-27 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,463,396 to Nishigaki (Nishigaki) in view of U.S. Patent No. 4,510,584 to Dias et al. (Dias) and in further view of U.S. Patent Application No. 2003/0063439 to Wei et al. (Wei). Claims 2 and 18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Nishigaki in view of Dias and Wei, and in further view of U.S. Patent No. 6,323,781 to Hutchison (Hutchison). Claims 4 and 20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Nishigaki in view of Dias and Wei, and in further view of U.S. Patent No. 6,411,531 to Nork et al. (Nork) and U.S. Patent No. 6,633,494 to Roohparvar et al. (Roohparvar). Claims 8 and 24 were rejected under 35 U.S.C. §103(a) as being unpatentable over Nishigaki in view of Dias and Wei, and in further view of U.S. Patent Application No. 2002/0144163 to Goodfellow et al. (Goodfellow). Claims 12-14 and 30 were rejected under 35 U.S.C. §103(a) as being unpatentable under 35 U.S.C. §103(a) as being unpatentable over Nishigaki in view of Dias and Wei, and in further view of non-patent literature "Switched-Capacitor DC-DC Converters for Low-Power On-Chip Applications" by Maksimovic et al. (Maksimovic).

Amendments to the Claims

Although Applicant respectfully disagrees with the rejections asserted in the Office Action based on the cited references, Applicant has nonetheless amended the claims so as to expedite prosecution by further emphasizing certain aspects in the claims. Applicant respectfully asserts, however, that the amendments should not be interpreted as the surrender of any subject matter. Applicant is not conceding by these amendments

that any previously submitted claims are not patentable over the references of record. Applicant's present claim amendments are only submitted for purposes of facilitating expeditious prosecution of the present Application. Accordingly, Applicant reserves the right to pursue any previously submitted claims in one or more continuation and/or divisional patent applications.

In this response, Applicant has amended the claims to emphasize certain aspects of the claims. In particular, Applicant has amended independent Claims 1 and 17 to further emphasize the operation and configuration of the claimed power supply integrated circuit (IC). Claims 1 and 17 now recite the further limitation that the processing circuitry in the IC includes both structure for modifying the input time varying signal and structure for scaling a modified input time varying signal based on a DC supply voltage received from the DC to DC converter portion of the IC. Such an amendment is fully supported throughout the Specification, as discussed below. No new subject matter has been introduced by these amendments.

Aspects of the Claims

Prior to discussing the cited references, it may be useful to discuss certain aspects of the claims. The claims, as typified by Claim 1 recite a power supply IC (100), as shown in FIGs. 1 and 2 (reproduced below).

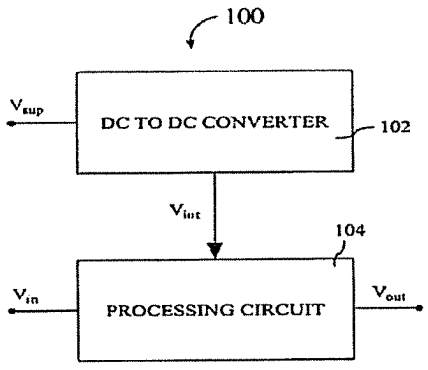


FIG. 1

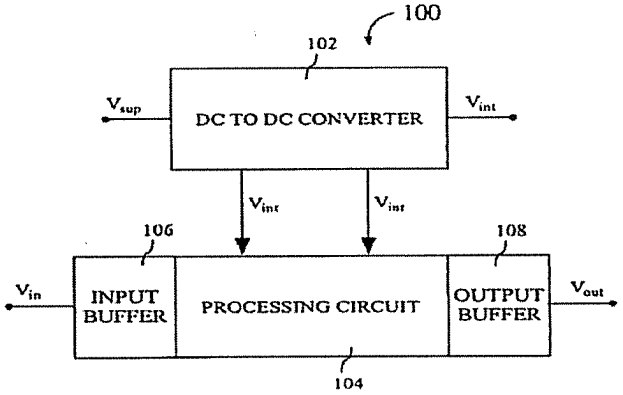


FIG. 2

The power supply IC (100) can receive a single DC supply voltage (Vsup) and at least one time-varying data signal (Vin), such as a radio frequency (RF) or microwave data signal. The power IC (100) comprises two portions, a DC to DC converter portion (102) and a translation or processing circuit (104) portion. As recited in the claims, at least one of the output voltages produced by the DC to DC converter can be used to power the processing circuit (104) portion.

The processing circuit portion (104) can include structure for executing two different tasks: (1) modification of the input time varying signal and (2) scaling of the modified time varying signal. To accomplish the first task, the processing circuit portion (104) includes structure for modifying at least one parameter of the input time varying signal. To accomplish the second task, the processing circuit portion (104) includes structure for scaling the modified time varying signal. This scaling is not fixed, but rather is dependent on the voltages output by the DC to DC converter portion (102). In other words, the scaling structure requires as input an output of the DC to DC converter portion (102) and the time varying signal, as shown below in FIGs. 5 and 6, the output (Vout) of the circuit for a processing circuit portion (500, 600) is completely dependent on the input supply voltage (Vsup) for the processing circuit portion:

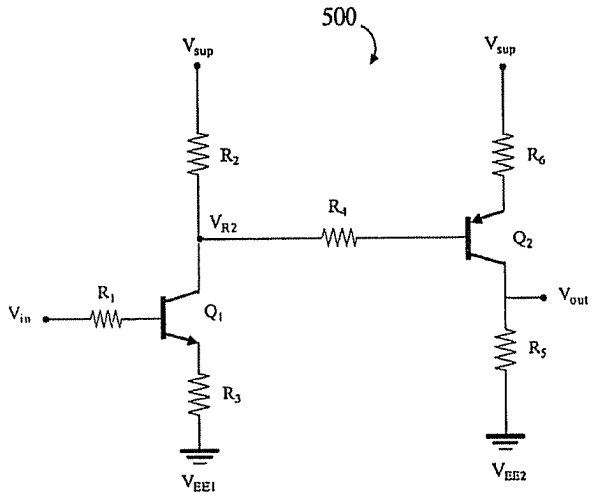


FIG. 5

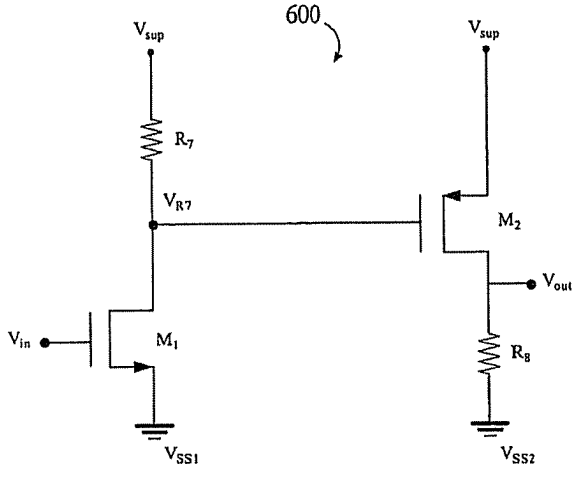


FIG. 6

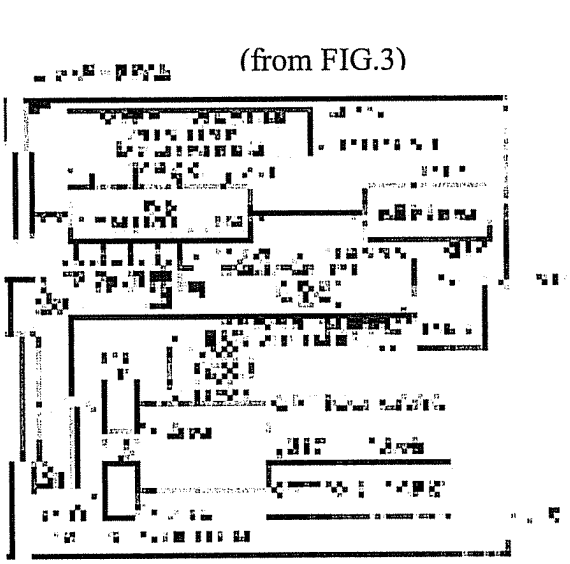
Therefore, the voltage level of Vout, regardless of the level of Vin, will always be dependent on Vsup, which is provided by the DC to DC converter portion, as recited in the claims.

The Claims Define Over the Cited References

In the Office Action, independent Claims 1 and 17 were rejected as being unpatentable over Nishigaki in view of Dias and Wei. Nishigaki discloses an apparatus for controlling internal heat generated for a computer system. Dias discloses a non-volatile random access memory cell. Wei discloses an integrated circuit. It is asserted in the Office Action that all the limitations of Claims 1 and 17, as previously submitted, were disclosed in Nishigaki, Dias, and Wei. However, in view of ***all*** the teachings of the cited references, Applicant respectfully submits that the claims, as amended, define over the references of record.

In particular, the cited references fail to disclose or suggest an integrated circuit configured to produce a plurality of DC supply voltages and that the time-varying input signal is scaled by one of these produced DC supply voltages. According to the Office Action, this is substantially, if not entirely disclosed in Nishigaki. In particular, the Office Action cites elements of FIGs. 3 and 4 (portions reproduced below) as disclosing these elements recited by the claims. Applicants respectfully disagree.

(from FIG.3)



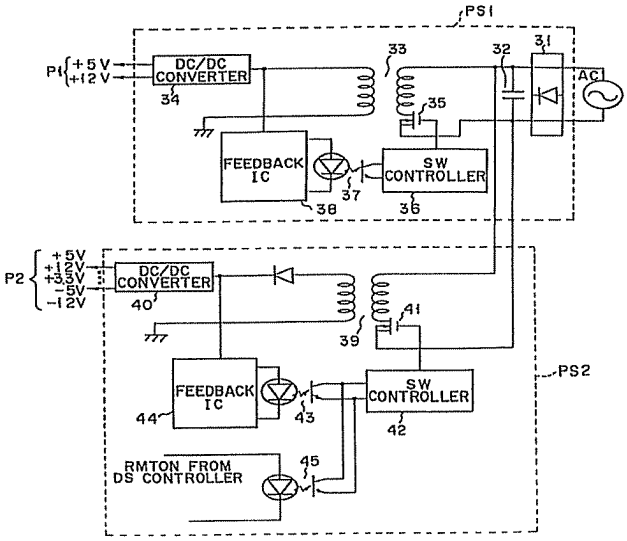


FIG. 4

As shown in FIG. 4, the DC/DC converter (34) of PS1 generates a plurality of output voltages (P1). The output voltages (P1) are input into the DS controller (211), as shown in FIG. 3. The DS controller (211) also receives VCC, which is asserted in the Office Action to be a time varying signal. Based on VCC and PS1, the DS controller (211) generates signal RTMON, which is fed into PS2. RTMON is then used in PS2 to generate time varying signals by essentially using RTMON to control when the DC/DC converter (40) in PS2 is turned on and off. However, Nishigaki fails to disclose or suggests that the voltage output level of DC/DC converter (40) in PS2 is related in any way to the voltage output levels of PS1. Rather, as the Office Action acknowledges on page 3, RTMON is an activation signal only and is only used to determine ***when*** the output voltage levels of DC/DC converter (40) are produced, ***not how*** RTMON should be scaled by DC/DC converter (40).

Furthermore, Nishigaki neither discloses nor suggests any structure to do so. Applicant respectfully points out that nowhere does Nishigaki disclose or suggest any voltage outputs from PS1 (P1) are provided to PS2. Rather, Nishigaki only discloses that DC/DC converter (40) operates completely independently of the voltage levels output from DC/DC converter (34). That is, the output voltage levels of PS2 are fixed and are independent of the voltage levels produced by PS1.

In contrast, the claims, as amended, explicitly recite that the output of the DC to DC converter is provided to the processing circuitry. Furthermore, this output is not only used to power the circuitry for modifying the input time varying signal, but is also used to determine to what output voltage level the output of the processing circuitry should be scaled. Therefore, the claims, as amended, recite an IC can not only provide a supply voltage to another IC, but can adjusting input signals to the voltage range appropriate for the other IC. For example, if the claimed IC is used to power a second IC requiring a supply voltage between 0 and 5 V and data signals also between 0 and 5 V, the claimed IC not only provides the correct supply, but can also using the supplied voltage output to scale the data signals to the appropriate range (0 and 5 volts). Such a configuration is

advantageous in that two DC to DC converters are no longer needed, as illustrated in Nishigaki. Only a single DC to DC converter is used, in conjunction with the scaling portion of the processing circuitry, to produce the time varying signal at the correct voltage level.

Accordingly, Nishigaki, Dias, and Wei, alone or in combination with any other reference of record, fail to disclose, suggest, or render obvious each and every element as recited in impendent Claims 1 and 17. Applicant therefore respectfully submits that the independent claims define over the references of record. Furthermore, as the remaining claims depend from one of Claims 1 and 17, while reciting additional features, Applicant also submits that the dependent claims likewise define over the references of record.

CONCLUSION

This application is now in full condition for allowance, which action is respectfully requested. Applicants request that the Examiner call the undersigned if clarification is needed on any matter within this Amendment, or if the Examiner believes a telephone interview would expedite the prosecution of the subject application to allowance.

Respectfully submitted,

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